MODELING A NEW GENERATION OF RF DEVICES: MOSFETs FOR L-BAND APPLICATIONS

Julio C. Costa, Dave Lovelace,Dave Ngo, and Natalino Camilleri
Semiconductor Products Sector, Motorola
2100 E. Elliot Road, EL609, Tempe Arizona 85284

Abstract: Results on large signal modeling efforts of a novel MOSFET technology for L-band RF applications will be presented. A parameter extraction procedure which yields accurate RF MOS large-signal models using DC and s-parameter data is presented along with a comparison of measured and modeled class-B amplifier, mixer and s-parameter data.

Introduction

The RF industry is currently actively pursuing the development of novel power MOSFET RF technologies for L band (0.39-1.55GHz) applications. The RF performance of these new MOS technologies at this frequency range is at par with that of Si Bipolar transistors and GaAs MESFETs, opening up new exciting possibilities in RF and digital/analog integration with CMOS technologies.[1] MOSFET technology is both simple and robust, which coupled with its excellent noise, power gain and linearity may make MOS devices major players in the portable communications market. Here, we describe the development and modeling efforts of an RF MOSFET model suitable for large signal computer-aided design. The extraction is validated by a comparison of model-versus-measured results of DC and s-parameter data, along with a matched amplifier and a Gilbert-cell mixer.

Extracting Large Signal Models for RF MOSFET devices

The RF MOSFET devices in our study were fabricated using a technology which features 1.5mm gate lengths, 400A oxide thicknesses and drain breakdown voltages in excess of 60 Volts. This technology typically yields FT values greater than 5GHz, FMAX values greater than 9 GHz, and a maximum stable gain greater than 17dB at 1GHz. The process makes use of custom doping profiles which enhance the lateral electric field profile of the device. These characteristics optimize the channel transconductance of the device while making it the transistor virtually immune to short-channel effects.

The electric field profile near the source of the device and the narrow gate lengths create a current mechanism which is quickly dominated by velocity-saturation of charge carriers as a function of the applied drain-source bias VDS. This yields a transconductance profile which departs from the traditional parabolic-shape dependence with gate voltage VGS. Our proposed RF model makes use of an existing SPICE Level 3 MOSFET[2] model coupled with two non-linear resistors in the source and drain to simulate some of the physical features of the device. The complete RF model is depicted in figure 1. The non-linear source and drain piece-wise linear resistors need to be included to accurately simulate the high current compression regime, which SPICE MOS models do not take into account. Without these elements, the RF output power is often overestimated due to a fictitiously high transconductance. The equations used in the Level 3 MOS model are essentially faster and more manageable semi-empirical simplifications of those in the more physical MOS Level 2 SPICE model, but yet fairly accurate with respect to short-channel and velocity-saturation effects. The Level 3 SPICE model must also be coupled with a separate capacitance model. In our case, we used the Ward-Dutton Charge Conservation Model[3] (currently implemented in most commercial SPICE packages as well in harmonic balance simulators such HP-MDS and HARMONICA) to model the gate-drain and gate-source capacitances as a function of bias, and a simple junction capacitance between drain and the substrate, which in our case is directly tied to the source by design. All of the parameters for our RF LDMOS model are optimized from DC and s-parameter measurements according to the methodology depicted in Fig.2:

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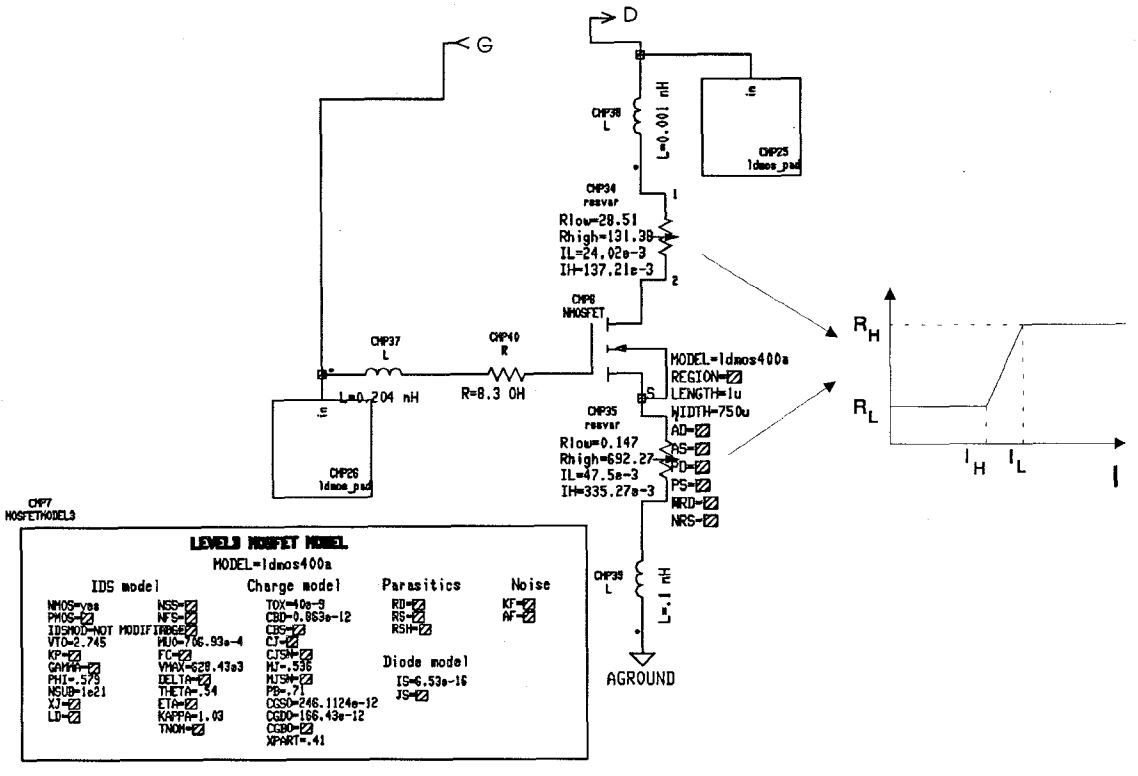

Fig. 1 : Complete RF LDMOS model as implemented in the harmonic balance simulator HP-MDS. The MOSFET transistor uses a simple SPICE level 3 MOS model with the parameters shown in the enclosed box. Two non-linear resistors must be added to the source and the drain to accurately simulate the high current compression regime of the LDMOS..

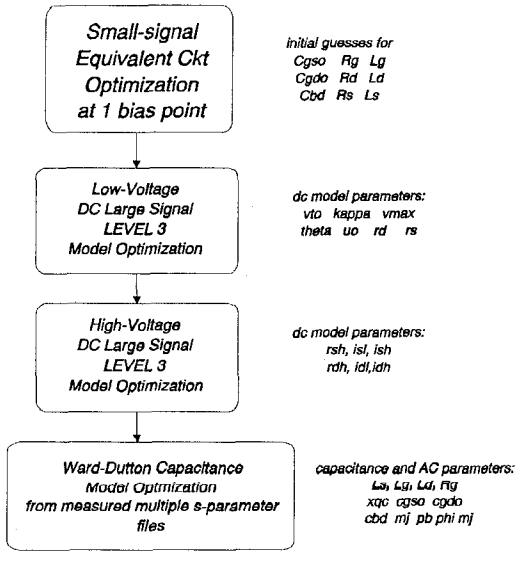

Fig. 2: Methodology of optimization of the RF LDMOS model parameters from DC and s-parameters measurements.

The technique consists of combining DC and s-parameter measurements in the range between 0.2GHz and 5 GHz using a vector network analyzer for appropriately chosen bias points. Initially, DC transfer characteristics (IDS versus VDS for different VGS) are measured; these DC measurements should include several points in the linear and weak inversion regime for a range of values of VGS from near pinch-off to a current value which encompasses the high-current compression regime. The s-parameters of the device are then measured for 6~7 different bias points; the choice of bias points should include several points in the saturation region and a few in the linear and weak-inversion regions in order to optimize the parameters of the capacitance model. For our parameter extraction, we used the optimizer included in the current HSPICE (META Software) simulator, although any circuit simulator which can handle s-parameter and Large-Signal modeling can in principle also be used. The parameter optimization then takes place as follows:

1) A small-signal FET 13-element equivalent circuit optimization is initially performed for s-parameter measurements taken at one bias point in the saturation region. This is a small-signal AC optimization which will only provide initial guesses for RG, RS, RD, LG, LS, LD, CGSO, CGDO, and CBD. These initial guesses will help the optimizer later when it handles a multi-bias optimization; without these initial guesses, the simulator might stall at a local minimum which is away from the optimum point.

2) Using initial guesses from 1) and geometrical data pertaining to the device, the low-voltage DC model parameters are allowed to optimize with respect to the measured DC data at lower gate biases (without current compression effects). We allow the initial guesses from 1) to vary only by +/- 25% of their original values. At the end of this optimization, the parameters VTO, KAPPA, VMAX, THETA, UO, RD and RS are obtained and will not be allowed to vary anymore.

3) Using the high current portion of the DC data set (where GM approaches zero), the remaining parameters for the non-linear resistors are optimized. We then obtain: RDH, IDL and IDH for the drain resistor and RSH, ISL and ISH for the source resistor.

4) Using the fixed DC parameters from 2) and 3) and the initial guesses from 1), the optimizer is allowed to optimize the capacitance model with respect to the measured s-parameters versus bias. At the end of this AC linear optimization, the full set of AC model parameters are obtained: RG, LG, LS, LD, CGSO, CGDO, CBD, PHI, MJ, PB and XQC.

Measured vs Modeled Results

DC AND S-PARAMETERS: Using the method outlined in the previous section, an RF model for a 1.5x750mm MOS transistor was extracted. Fig. 3 depicts the DC and s-parameter agreement for two different biases. The DC characteristics are accurately described by the model well into the very high current/voltage regime, where thermal effects affect the measurements (negative output conductances in the measured currents). We also show s-parameter comparisons between measured and modeled data for biases in the linear and saturation regions. The discrepancies occur mainly in the linear range of the current, where the charge-conservation capacitance model somewhat underestimates the device capacitances.

MATCHED AMPLIFIER : The proposed model was also used to simulate the RF performance of a matched class-B amplifier at different quiescent points at 850MHz. Figure 4 depicts the results of a simulation at VD=12.5V and IDQ=3mA using standard line tuners for the input and output matches. The simulations were performed using the time-domain simulator HSPICE.

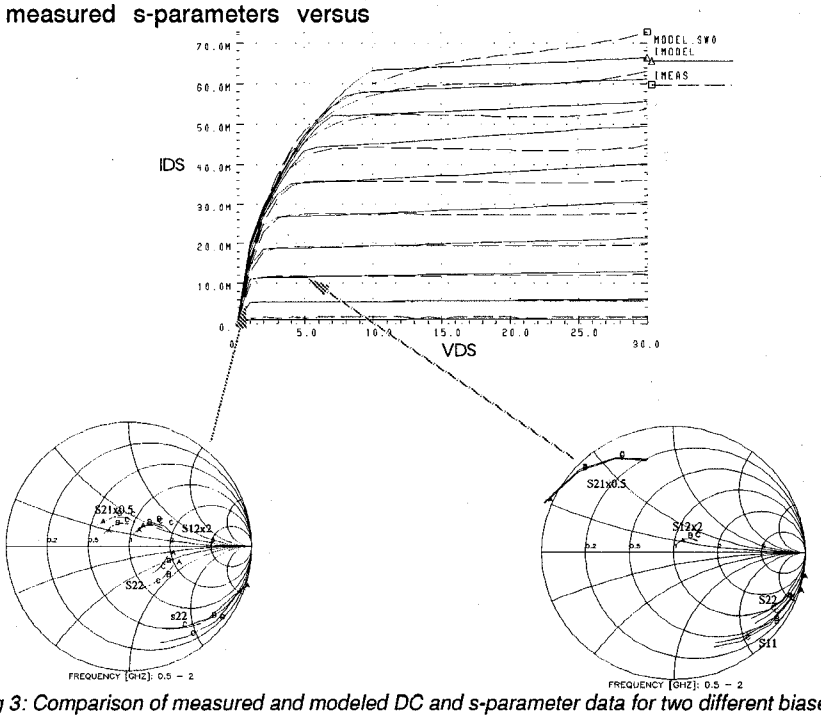

Fig 3: Comparison of measured and modeled DC and s-parameter data for two different biases.

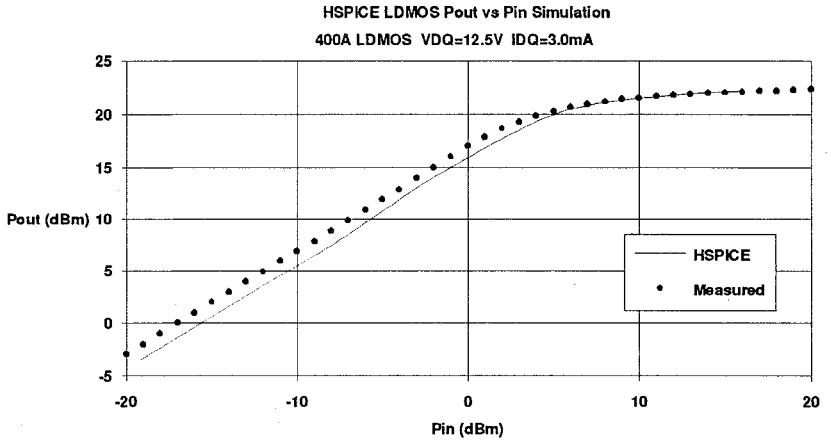

Fig. 4: Measured and modeled fundamental Output Power versus Input Power for a matched MOSFET amplifier at 850MHz. The device width is 750mm. Line tuners are used for both input and output matches.

GILBERT-CELL MIXER : The MOSFET RF model was also utilized in the simulation of a low current 900MHz Gilbert cell mixer. The mixer operates at a bias supply of 5V and 5mA. The circuit schematic of the mixer is depicted in Fig. 5. The circuit was modeled using the harmonic balance simulator HP-MDS. The measured and simulated conversion gain (GC) versus LO drive power characteristics of the Gilbert cell mixer are shown in Fig. 6. The discrepancies between the measured and modeled data arise mostly from the assumed losses in the transformers and baluns, which at this time have not been fully characterized. The overall agreement, however, is adequate and correctly predicts the LO power level near the 1-dB gain compression regime of the mixer, which indicates that the large-signal characteristics of the device are being adequately simulated by the model.

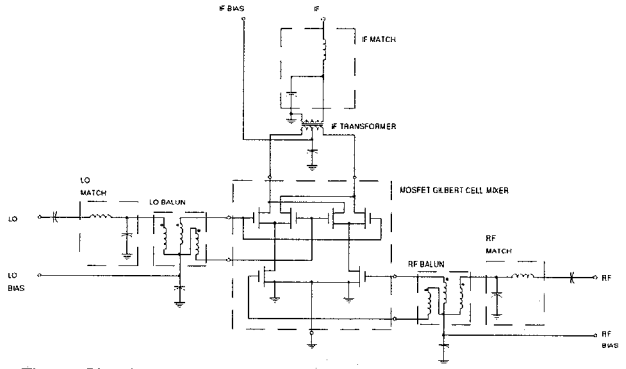

Fig. 5: Circuit topology of the low-current Gilbert cell mixer.

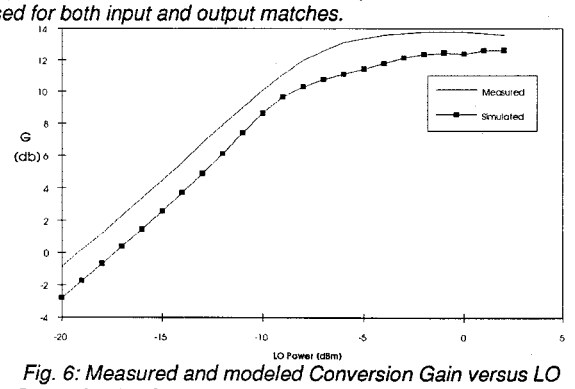

Fig. 6: Measured and modeled Conversion Gain versus LO Power for the Gilbert cell mixer at VD=5V and ID=5mA. The LO frequency was F(LO)=785MHz, the RF frequencies were F(RF1)=860MHz and F(RF2)=860.025MHz.

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[1]see for example: I. Yoshida, M. Katsueda, S. Ohtaka, Y. Maruyama, and T. Okabe, *Proc. Intern. Symposium on Power Semiconductor Devices and ICs*, Tokyo, pp156-7 (1992).; or H. Itoh, T. Okabe, M. Nagata, *Proc. of the IEEE IEDM*, pp.95-96 (1983).

[2]P. Antognetti, and G. Massobrio, Semiconductor Device Modeling with Spice, McGraw-Hill, New York (1987).

[3]D. Ward, and R. Dutton, *IEEE J. of Solid State Circuits*, Vol. 13, pp.703-707 (1978).